REMARKS

Claims 1, 2-6, 8-18 and 20-22 are pending in the present application, were examined, and stand rejected. In response, Claims 1, 10, 14, 16 and 18 are amended, Claim 13 is cancelled and Claims 23-28 are added. Applicants respectfully request reconsideration of pending Claims 1, 2-6, 8-12, 15-18 and 20-28 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 1, 3-6, 8-18 and 20-22 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,148,384 issued to Devanagundy et al. ("Devanagundy"). Applicants respectfully traverse this rejection.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik v. American Hoist & Derrick* ("Lindemann"), *730 F.2d 452, 1458 (Fed. Cir. 1994)*(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. *Titanium Metals Corp. of American v. Banner* ("Banner Titanium"), *778 F.2d 775, 777 (Fed. Cir. 1985).*

Regarding Claim 1, Claim 1 is amended to remove redundant claim language regarding the revision identification register. Claim 1 recites the following features, which are not disclosed by Devanagundy or the references of record:

> a revision identification register to store a revision identification value of the apparatus, and
>
> a revision identification modification register, the revision identification modification register to allow modification of the revision identification register contents when indicated by the contents of the revision identification modification register. (Emphasis added.)

Conversely, Devanagundy teaches:

> A control register containing one or more protection bits/flags which correspond to portions of an attached SEEPROM. A protection bit in the control register being set prevents writing or erasing of the corresponding portion of the SEEPROM. Thus, setting protection bits protects corresponding portions of the SEEPROM from write and erase operations. Furthermore, software cannot change the protection bits unless the bus device is in a specific state, for example, a state corresponding to a target abort according to the PCI bus protocol. (col. 3, lines 25–34.) (Emphasis added.)

As further described by Devanagundy :

> In the exemplary embodiment, SEEPROM 144 is a 1-Kbit memory, such as a 93C46 or 93C66 available from Atmel, Inc. that stores a worldwide web port and node name, a local address, a subsystem-ID, a subsystem vendor ID and a preferred

FC port address, size information for memory 146, and other board related data. (col. 4, lines 33-38.) (Emphasis added.)

Based on the cited passage above, SEEPROM 144, as taught by Devanagundy fails to include either a revision identification register or a revision identification modification register, the contents of which determine whether the revision identification register is enabled to allow modification thereof. Devanagundy teaches a SEEPROM that stores information including a subsystem ID and a subsystem vendor ID with one or more associated protection bits/flags to enable protection of corresponding portions of the SEEPROM (*See*, col. 3, lines 25-34). However, Devanagundy's failure to disclose or suggest a SEEPROM including a revision identification value of an apparatus, as recited by Claim 1, prohibits the Examiner from establishing the disclosure of the revision identification modification register to allow modification of a revision identification value within the revision identification register, as recited by Claim 1.

FIG. 2 of Devanagundy further illustrates host adapter 140, as shown in FIG. 1. As illustrated, host adapter 140 includes a host interface including configuration registers (CONFIG. REGS. 218). As known to those skilled in the art, the Peripheral Component Interconnect Local Bus Specification, Rev. 2.2, released December 18, 1998, added a subsystem vendor ID register and a subsystem ID register to the configuration registers provided by a PCI device. As indicated by the PCI Bus Specification Rev. 2.2, the configuration registers include a revision identification register that generally stores an 8-bit revision identification value assigned by a device manufacturer to indicate a revision number of a device.

Applicants respectfully submit that SEEPROM 144, as taught by Devanagundy, does not store a revision identification value and therefore fails to teach a revision identification register, as required by the PCI Bus Specification Rev. 2.2 or a revision identification modification register, as recited by Claim 1. Applicants respectfully submit that, as dictated by the PCI Bus Specification, the revision identification register would be contained within configuration registers 218, as shown in FIG. 2 of Devanagundy.

Furthermore, as explicitly required by Devanagundy,

> software cannot change the protection bits unless the bus device is in a specific state, for example, a state corresponding to a target abort according to the PCI bus protocol. (col. 3, lines 31–34.) (Emphasis added.)

Conversely, modification of the revision identification register, as recited by claim 1, is based solely on the contents of the revision identification modification register regardless of a state of the apparatus, as recited by Claim 1.

Accordingly, Applicants respectfully submit that Devanagundy fails to disclose:

> A revision identification modification register to allow modification of the value within the revision identification register when indicated by the contents of the revision modification register, as recited by Claim 1. (Emphasis added.)

The case law establishes that each and every element of a claim must be exactly disclosed and in the anticipatory reference to establish a *prima facie* case of anticipation. Id. Here, Applicants respectfully submit that Devanagundy is not a proper anticipatory reference under §102(b), since Devanagundy fails to disclose a revision identification register having a revision identification modification register associated with the revision identification register to allow modification of a value within the revision identification register, as recited by Claim 1.

Consequently, Applicants respectfully submit that the Examiner is prohibited from establishing a *prima facie* case of anticipation of Claim 1 under §102(b) if Devanagundy is used as anticipatory reference. Therefore, Applicants respectfully submit that Claim 1 is patentable over Devanagundy, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 1.

Regarding Claims 2-5, Claims 2-5, based on their dependency from Claim 1, are also patentable over Devanagundy, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 2-5.

Regarding Claim 18, Claim 18 recites a system including a system logic device, including a revision identification register and an associated revision identification modification register, to allow modification of the value within the revision identification register when indicated by the contents of the revision identification modification register. Furthermore, Claim 18 recites:

> a non-volatile memory to store a pre-operating system software agent, the pre-operating software agent to determine whether to modify a value stored in a revision identification register to indicate a first device stepping. (Emphasis added.)

For at least the reasons described above with reference to Claim 1, Devanagundy is not a proper anticipatory reference under §102(b) to render Claim 18, as amended, unpatentable since Devanagundy fails to disclose a revision identification modification register associated with a revision identification register, where the contents of the revision identification modification register indicate whether to allow modification of a value within the revision identification register.

Accordingly, for at least the reasons described above, Applicants respectfully submit that Applicants' amendments to Claim 18 prohibit the Examiner from establishing a *prima facie* case of anticipation of Claim 18, based on Devanagundy as an anticipatory reference, since Devanagundy fails to disclose the revision identification modification register, as recited by Claim 18. Therefore, Applicants respectfully submit that Claim 18, as amended, is patentable over Devanagundy, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 18, as amended.

Regarding Claims 20-22, Claims 20-22, based on their dependency from Claim 18, are also patentable over Devanagundy, as well as the references of record. Consequently, Applicants

respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 20–22.

Regarding Claims 6 and 12, Claims 6 and 12 recite the following claim features, which are not disclosed by either Devanagundy or the references of record:

> ensuring that a revision identification modification register contains a value that indicates that the revision identification register will accept writes; and
>
> replacing the current value with a revision identification value that indicates the first device stepping if the revision identification of the device does not indicate the first device stepping. (Emphasis added.)

As indicated above with reference to Claims 1 and 18, Devanagundy fails to disclose a revision identification register having an associated revision identification modification register that contains a value that indicates whether the revision identification register will accept writes. The bus device, as taught by Devanagundy, operates according to a PCI bus protocol. (*See*, col. 3, lines 30-33.) As a result, the SEEPROM, as taught by Devanagundy does not include a revision identification value, since a revision identification value would be stored within a revision identification register, as required by the PCI Bus Specification, such as, for example, PCI Bus Specification Rev. 2.2.

Hence, as dictated by the PCI bus protocol, the bus device taught by Devanagundy includes a revision identification register within CONFIG. REGS. 218, as shown in FIG. 2 of Devanagundy. However, Devanagundy fails to disclose any teachings regarding protection of the revision identification register contents. As a result, Devanagundy fails to teach a revision identification modification register associated with the revision identification register, as recited by Claims 6 and 12.

Accordingly, Applicants respectfully submit that the features of Claims 6 and 12 prohibit the Examiner from establishing a *prima facie* case of anticipation of Claims 6 and 12 with Devanagundy as an anticipatory reference, since Devanagundy fails to disclose a revision identification modification register, where contents of a revision identification modification register indicates whether the revision identification register will accept writes.

Consequently, Applicants respectfully submit that Claims 6 and 12 are patentable over Devanagundy, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 6 and 12.

Regarding Claim 8, Claim 8 is patentable over Devanagundy, as well as the references of record, based on its dependency from Claim 6. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 8.

Regarding Claim 14, Claim 14 is patentable over Devanagundy, as well as the references of record, based on its dependency from Claim 12. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 14.

Regarding Claims 9 and 15, Claims 9 and 15 recite the following claim feature, which is neither disclosed nor suggested by either Devanagundy or the references of record:

> executing a pre-operating system software agent, the pre-operating software agent to determine whether to modify a value stored in a revision identification register;
>
> modifying the value stored in the revision identification register if modification of the revision identification register is enabled according to contents of the revision identification modification register. (Emphasis added.)

As described by Devanagundy:

> [W]riting to a protected portion of the SEEPROM requests: starting a dummy SEEPROM access; causing a PCI target abort; clearing a protection bit to unprotect a corresponding portion of the SEEPROM; and writing to the unprotected portion of the SEEPROM once the dummy access is complete. Causing a PCI target abort during another access of the SEEPROM and setting the appropriate protection bit protects the new information from further changes. The combination of generating of a target abort during an SEEPROM access and changing a protection bit during the target abort provides a passkey for changing information in a protected portion of memory. (col. 3, lines 37-48.)

As indicated by the cited passage above, writing to the protected portion of the SEEPROM does not involve a pre-operating system software agent, which determines whether to modify a value stored in a revision identification register, as recited by Claims 9 and 15. Conversely, Devanagundy teaches:

> Protocol engine 250 or host computer 110 executes software which initiates a read, write, or erase operation to SEEPROM 144 via SEEPROM interface 320. (col. 6, lines 51-54.)

Applicants respectfully submit that the execution of such software to initiate a read, write or erase operation to SEEPROM 144 occurs following activity by any pre-operating system software agent and, in fact, occurs following loading of the operating system. Hence, Applicants respectfully submit that the Examiner is prohibited from illustrating the disclosure within Devanagundy of a pre-operating system software agent to determine whether to modify a value stored in a revision identification register, as recited by Claims 9 and 15.

Furthermore, as indicated above regarding Claims 5 and 12, Devanagundy fails to disclose a revision identification register having a revision identification modification register, the contents of which determine whether modification of the revision identification register is enabled. As indicated above, the SEEPROM, as taught by Devanagundy, does not include a revision identification value since such information is stored as a revision identification register, as recited by the PCI bus protocol, such as, for example, PCI Bus Specification Rev. 2.2. Such a revision identification register would be contained within CONFIG. REGS. 218, as shown in FIG. 2 of Devanagundy, since the bus device taught by Devanagundy operates according to a PCI bus protocol. (*See*, Devanagundy, col. 3, lines 33-34.)

Applicants respectfully submit that the above features of Claims 9 and 15 prohibit the Examiner from establishing a *prima facie* case of anticipation of Claims 9 and 15 under §102(b) with Devanagundy as an anticipatory reference, since Devanagundy fails to disclose or suggest a revision identification register having an associated revision identification modification register that determines whether a revision identification value within the revision identification register is modifiable.

Accordingly, Applicants respectfully submit that Claims 9 and 15 are patentable over Devanagundy, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 9 and 15.

Regarding Claims 10 and 11, Claims 10 and 11, based on their dependency from Claim 9, are also patentable over Devanagundy, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 10 and 11.

Regarding Claims 16 and 17, Claims 16 and 17, based on their dependency from Claim 15, are also patentable over Devanagundy, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 16 and 17.

Regarding new Claims 23, 27 and 28, new Claims 23, 27 and 28 are patentable over Devanagundy, as well as the references of record, since Claims 23, 27 and 28 recite features regarding a revision identification register having an associated revision identification modification register that contains a value that indicates whether the revision identification register will accept writes. Accordingly, Applicants respectfully request that the Examiner allow new Claims 23, 27 and 28, as well as Claims 24-26, based on their dependency from Claim 23.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1, 2-6, 8-12, 15-18 and 20-28, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: March 28, 2005

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 28, 2005

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Marilyn Bass March 28,2004